



SHEET 1 OF 11

INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.  
**043876-0147**SERIAL NO.  
**10/705,946**APPLICANT  
**HANSEN, C., et al.**FILING DATE  
**November 13, 2003**GROUP  
**2183**

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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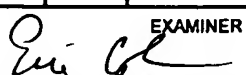
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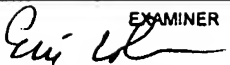
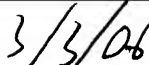
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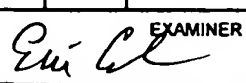
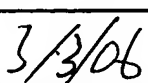
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<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>		<b>ATTY. DOCKET NO.</b> <b>043876-0147</b>	<b>SERIAL NO.</b> <b>10/705,946</b>
		<b>APPLICANT</b> <b>HANSEN, C., et al.</b>	
		<b>FILING DATE</b> <b>November 13, 2003</b>	<b>GROUP</b> <b>2183</b>
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<b>EXAMINER'S INITIALS</b>	<b>CITE NO.</b>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
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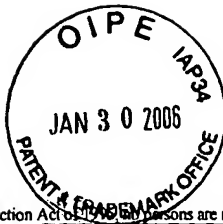
<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  (PTO-1449)		ATTY. DOCKET NO. <b>043876-0147</b>	SERIAL NO. <b>10/705,946</b>
		APPLICANT <b>HANSEN, C., et al.</b>	
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E.C.	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
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<b>(Suppl.) INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>				<b>ATTY. DOCKET NO.</b> <b>43876-147</b>		<b>SERIAL NO.</b> <b>C ntinuati n f Serial No.</b> <b>10/436,340</b>	
				<b>APPLICANT</b> <b>Craig HANSEN, et al.</b>			
				<b>FILING DATE</b> <b>November 13, 2003</b>		<b>GROUP</b> <b>To be assigned</b>	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codez (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
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		<b>EXAMINER</b> <div style="display: flex; justify-content: space-between; align-items: center;"> <span style="font-size: 1.5em;">3/3/06</span> <span>DATE CONSIDERED</span> </div>					

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Application Number	10/705 946	
			Filing Date	November 13, 2003	
			First Named Inventor	Craig C. HANSEN, et al.	
			Group Art Unit	2183	
			Examiner Name	CHAN, EDDIE P	
Sheet	1	of	10	Attorney Docket Number	43876-147

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
EC	AT	WO 93/11500				


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				Application Number	10/705,946
				Filing Date	November 13, 2003
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
Examiner Name	CHAN, EDDIE P				
Attorney Docket Number	43876-147				
Sheet	2	of	10		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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EL	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
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	BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167)	
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				First Named Inventor	Craig C. HANSEN, et al.
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Sheet	3	of	10	Attorney Docket Number	43876-147

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		Number-Kind Code <sup>2</sup> (if known)			
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	BP	US-5,721,892	02/24/1998	Peleg, et al.	
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	BS	US-5,768,546	06/16/1998	Kwon	
	BT	US-5,887,183	03/23/1999	Agarwal, et al.	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				

Examiner Signature	<i>Eui Ch</i>	Date Considered	3/3/06
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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/705,946
				Filing Date	November 13, 2003
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
Examiner Name	CHAN, EDDIE P				
Sheet	4	of	10	Attorney Docket Number	43876-147

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T <sup>2</sup>
EC	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
	BZ	Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 – 590)	
	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141)	
	CB	PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 – 176)	
	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 – 776)	
	CD	Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 – 751)	
	CF	Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 – 763)	
	CG	Nikhil et al., "T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 – 476)	
	CH	Papadopoulos et al., "T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 – 289)	
	CI	Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 – 262)	
	CJ	M. Phillip, "Performance Issues for 88110 RISC Microprocessor," IEEE, 1992 (51056DOC008752 – 757)	
	CK	M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 – 789)	
	CL	R. Mueller, "The MC88110 Instruction Sequencer," Northcon, 1992 (51056DOC009735 – 738)	
	CM	J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 – 742)	
	CN	K. Pepe, "The MC88110's High Performance Load/Store Unit," Northcon, 1992 (51056DOC009743 – 747)	
	CO	J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 – 063)	
	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 – 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 – 656)	
	CS	Awaga et al., "The $\mu$ VP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
EC	CT	Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 – 812)	

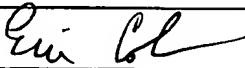
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		First Named Inventor	Craig C. HANSEN, et al.		
		Group Art Unit	2183		
		Examiner Name	CHAN, EDDIE P		
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CC	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194)			
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 - 607)			
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)			
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 - 034)			
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279)			
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)			
	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)			
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 - 607)			
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918)			
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)			
	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)			
	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)			
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)			
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)			
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)			
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)			
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)			
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)			
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)			
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510)			
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)			
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 - 443)			
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 - 459)			
	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 - 5299)			
CC	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)			

Examiner Signature		Dated Considered	3/3/06
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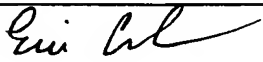
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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application Number	10/705 946
		Filing Date	November 13, 2003
		First Named Inventor	Craig C. HANSEN, et al.
		Group Art Unit	2183
		Examiner Name	CHAN, EDDIE P
		Attorney Docket Number	43876-147
Sheet	6	of	10

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T <sup>2</sup>
EC	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 - 666)	
	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 - 717)	
	DX	Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 - 710)	
	DY	Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 - 094)	
	DZ	Kohn et al., "A New Microprocessor with Vector Processing Capabilities," Electro/89 Conference Record, pp. 1-6 (April 11-13, 1989) (5156DOC070672 - 678)	
	EA	Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 - 642)	
	EB	Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 - 336)	
	EC	Margulis, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 - 7265 and 5156DOC069971 - 70626)	
	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 - 700)	
	EE	Patel et al., "Architectural Features of the i860 - Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 - 684)	
	EF	Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 - 647)	
	EG	Perry, "Intel's Secret is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 - 654)	
	EH	Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 - 101)	
	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 - 427)	
	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 - 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 - 73027)	
	EQ	Hansen, "Architecture of a Broadband MediaProcessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 - 283 and 51057DOC001825 - 831)	
EC	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 - 630)	


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				Filing Date	November 13, 2003
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				Group Art Unit	2183
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EC	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 - 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 - 923)	
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 - 040)	
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 - 300)	
	EW	Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 - 645)	
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, <a href="http://www.cs.wisc.edu/condor/doc/WiscIdeas.html">http://www.cs.wisc.edu/condor/doc/WiscIdeas.html</a> (1993) (51056DOC068704 - 711)	
	EY	Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 - 929)	
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
	FA	Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)	
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 - 673)	
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662)	
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028)	
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)	
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 - II-524 (April 1994) (51056DOC003070 - 073)	
	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 - 327)	
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 - 942)	
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)	
	FJ	Litzkow et al., "Condor - A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 - 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 - 628)	
	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 - 471)	
EC	FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 - 942)	

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el	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 - 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 - 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110-118) (51056DOC002949 - 957)	
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 - 896)	
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 - 946)	
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 - 609)	
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)	
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	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
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Examiner Signature	<i>Eui Gil</i>	Dated Considered	3/3/06
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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/705,946
				Filing Date	November 13, 2003
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	9	of	10	Attorney Docket Number	43876-147

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T <sup>2</sup>
EC	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (S1056DOC019304 - 323)	
		Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for <i>Inter Partes</i> Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	
	GQ	Deposition of Larry Mennermeier on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, "Intel Announces Record Revenue of 9.96 Billion", October 18, 2005	
	GT	The New York Times Article, "Intel Posts 5% Profit Increase on Demand for Notebook Chips", October 19, 2005	
	GU	USA Today Article, "Intel's Revenue Grew 18% In Robust Quarter for Tech", October 19, 2005	
	GV	The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005	
EL	GW	The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005	

Examiner Signature	<i>Eun CL</i>	Dated Considered	3/3/06
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# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.  
**043876-0147**

SERIAL NO.  
**10/705,946**

APPLICANT  
**Craig HANSEN, et al.**

FILING DATE  
**November 13, 2003**

GROUP  
**2183**

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CC	A	US 6,643,765	11-04-2003	Hansen et al.	
CC	B	US 6,725,356	04-20-2004	Hansen et al.	
		US			
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## FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
CC	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)
CC	D	Intel Press Release, "Intel Announces Record Revenue of \$9.96 Billion," Santa Clara, CA, 10-18-2005


EXAMINER  
*Eui CC*

3/3/06

DATE CONSIDERED

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>				<b>ATTY. DOCKET NO.</b> 43876-147		<b>SERIAL NO.</b> Continuation of Application No. 10/436,340	
				<b>APPLICANT</b> Craig HANSEN, et al.			
				<b>FILING DATE</b> November 13, 2003		<b>GROUP</b> To be assigned	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
cc		US 4,876,660	10/24/89	Owen et al.			
		US 4,956,801	09/11/90	Priem et al.			
		US 4,969,118	11/06/90	Montoye et al.			
		US 5,032,865	07/16/91	Schlunt			
		US 5,408,581	04/18/95	Suzuki et al.			
		US 5,500,811	03/19/96	Corry			
		US 5,557,724	9/17/1996	Sampat et al.			
		US 5,588,152	12/24/1996	Dapp et al.			
		US 5,640,543	6/17/1997	Farrell et al.			
		US 5,757,432	5/26/1998	Dulong et al.			
		US 5,802,336	9/1/1998	Peleg et al.			
		US 5,809,292	9/15/1998	Wilkinson et al.			
		US 5,818,739	10/6/1998	Peleg et al.			
cc		US 5,825,677	10/20/1998	Agarwal et al.			
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number -Kind Codes (if known)	Publication Date MY Y	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
cc		EP 0474246 A2	9/6/1991				
cc		EP 0654733 A1	7/5/1994				
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
cc		L. Kohn et al. "The Visual Instruction Set (VIS) in UltraSPARC" IEEE. 1995. 462-469.					
		D. Shaver. "A General-Purpose Array Processor for Seismic Processing" (Nov - Dec 1984) January - March 1998. 15th Anniversary Issue. 5-26.					
		R. Lee. "Accelerating Multimedia with Enhanced Microprocessors" IEEE Micro. April 1995. 22-32.					
		N. Margulis. "i860 Microprocessor Architecture" 1990. 8-10, 171-175, 182-183.					
cc		A. Levinthal et al. "Parallel Computers for Graphics Applications" 1987. 193-198.					
<b>EXAMINER</b> 				<b>DATE CONSIDERED</b> 3/3/06			

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		<b>APPLICANT</b> <b>Craig HANSEN, et al.</b>			
		<b>FILING DATE</b> <b>November 13, 2003</b>		<b>GROUP</b> <b>To be assigned</b>	

U.S. PATENT DOCUMENTS					
EXAMINER'S INITIALS	CITE NO.	Docmen Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC		US 5,835,782	11/10/1998	Lin et al.	
		US 5,886,732	3/23/1999	Humpleman	
		US 5,922,066	7/13/1999	Cho et al.	
		US 5,983,257	11/9/1999	Dulong et al.	
		US 6,016,538	1/18/2000	Gutttag et al.	
		US 6,092,094	7/18/2000	Ireton	
		US 6,401,194 B1	6/4/2002	Nguyen et al.	
		US 4,025,772	5/24/1977	Constant	
		US 4,489,393	12/18/1984	Kawahara, et al.	
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		US 4,893,267	1/9/1990	Alsop et al.	
		US 4,975,868	12/4/1990	Freerksen	
EC		US 5,157,388	10/20/1992	Kohn	

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						<div style="display: flex; justify-content: space-between;"> <span>Yes</span> <span>No</span> </div>

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
EC		K. Diefendorff et al. "Organization of the Motorola 88110 Superscalar RISC Microprocessor" IEEE Micro. April 1992. 40-63.
EC		L. Gwennap. "IBM Regains Performance Lead with Power2" Microprocessor Report. October 4, 1993. Vol. 7. No. 13. 1,6-10.
EC		L. Gwennap. "IBM Creates Power PC Processors for AS/400" Microprocessor Report. July 31, 1995. 15-16.

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		APPLICANT <b>Craig HANSEN, et al.</b>			
		FILING DATE <b>November 13, 2003</b>		GROUP <b>To be assigned</b>	

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CC		US 5,201,056	4/6/1993	Daniel et al.		
		US 5,268,855	12/7/1993	Mason et al.		
		US 5,268,995	12/7/1993	Diefendorff et al.		
		US 5,423,051	6/6/1995	Fuller et al.		
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		US 5,666,298	9/9/1997	Peleg et al.		
		US 5,669,010	9/16/1997	Duluk, Jr.		
		US 5,673,407	9/30/1997	Poland et al.		
		US 5,675,526	10/7/1997	Peleg et al.		
		US 5,680,338	10/21/1997	Agarwal et al.		
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						Yes      No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
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